B. Tech Degree III Semester Examination November 2010

CS 302 LOGIC DESIGN

(2006 Scheme)

Time : 3 Hours | Maximum Marks : 100

PART – A

(Answer ***ALL*** questions) (8 x 5=40)

I. (a) Perform the following conversions

(i) $(3.65.4)_{10} = (\quad)_2$ (2)

(ii) $(87B.6)_{16} = (\quad)_{10}$ (2)

(iii) $(1001)_{BCD} = (\quad)_{Excess\,3}$ (1)

(b) Which are universal gates? Why they are called so? Implement AND,OR,NOT gates using one universal gate. (5)

(c) Explain carry look ahead adder. (5)

(d) Implement the expression using minimum number of NAND gates $Y = (A + BC)(B + \bar{C}A)$. (5)

(e) How will you convert RS flip flop into JK flip flop? (5)

(f) What is race around condition? (5)

(g) Write notes on :

(i) fan in
(ii) fan out
(iii) propagation delay
(iv) power dissipation
(v) noise margin

(5)

(h) Explain CMOS, NAND and NOR gates with circuit diagrams. (5)

PART B (4 x 15 =60)

II. Implement (i) $f_1(A,B.C.D) = \sum m(0,1,2,3,10,11,14,15)$

(ii) $f_2(A,B.C.D) = \sum m(0,1,2,3,5,7,8,9,11)$

using minimum number of gates. (15)

OR

III. (a) Implement 1's complement and 2's complement arithmetic with examples. (7)

(b) Convert SOP to POS and POS to SOP expressions. (8)

IV. Write notes on :

(i) multiplexer (8)
(ii) demultiplexer (7)

OR

V. Explain PLA and PAL architecture. What are their applications? (15)

VI. What are different types of flipflops? Write down the truth table and excitation tables (RS,JK,MS-JR,D,T). (15)

OR

VII. (a) Design a serial in parallel out shift register. (7)

(b) Design and implement RING Counter. (8)

VIII. Explain following logic families.

(i) RTL (7)
(ii) TTL (8)

OR

IX. (a) Explain how CMOS to TTL interfacing can be done. (8)

(b) Explain DTL logic family. (7)

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