

FRAM71B Detailed Configuration Examples

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1 Introduction

This configuration procedure is my personal configuration of the FRAM71B. I tried more than those described in this document, but these are my favorites. Most of the helpful description and documentation are available on the forum:

- FRAM71B summary site: <https://www.hpmuseum.org/forum/thread-16219.html>
- FRAM71B User Manual: <http://www.hpmuseum.org/forum/attachment.php?aid=3958>
- FRAM-Toolkit: <https://www.hpmuseum.org/forum/thread-16175.html>
- FRAM71 Configuration Example (Intermediate Level): <http://www.hpmuseum.org/forum/thread-5068.html?highlight=FRAM71B>
- Configuration examples: <http://www.hpmuseum.org/forum/thread-6287-page-2.html?highlight=pyILPER>
- ROMCOPY documentation: <http://hhuc.us/2014/files/Speakers/08,09%20Joseph%20Horn/Online%20LIF%20Disk%20Project/SWAP/SWAP11/RCOPYDOC.txt> and <https://drive.google.com/file/d/0B-GPxmpKVCV0bU1zcjZX0GgwcVk/view>
- Bank Switching: <http://www.hpmuseum.org/forum/thread-6973.html?highlight=FRAM71+Bank>
- FRAM71B - Denver presentation 2016: http://hhuc.us/2016/files/Speakers/Bob_Proserpi/Presentation/HHC16_FRAM71B.pdf
- Soft Configuration Enhances Flexibility of Handheld Computer Memory: <http://www.hpmuseum.org/journals/71b.htm>

And it is worth the time to study the several documents. So I made my personal setup out of this great documentations, proposals and work of enthusiasts. Without their support and patience, especially – Sylvain Cote, Dave Frederickson, Bob Proserpi, Hans Brueggemann, Christoph Giesselink – I would not be able to do this work in this time.

This step by step instruction is based on the use of pyILPER, the PIL-Box and a MacBook Pro. I have tried to make the documentation carefully. However, there is no guarantee that the FRAM71B, HP71B or its components will be damaged. Sorry for my bad english too.

2 Mac OSX and PIL-Box

The easiest way to connect the HP71B with a computer is through the PIL-Box and in the case of Mac OSX or LINUX do it with pyILPER. I used MINICONDA to install the python programm – download via their website <https://docs.conda.io/en/latest/miniconda.html>. The python installation is straight forward and easy.

Download pyILPER <https://github.com/bug400/pyILPER> and go through the installation instructions on <https://github.com/bug400/pyilper/blob/master/INSTALL.md>.

Don't forget to run the update sequence in the terminal window: `conda update --all` and at the first time: `conda config --add channels bug400` for Updates: `conda install pyilper`

Update pyILPER to 1.8.5 in terminal window with: `conda install python=3.6` see <https://www.hpmuseum.org/forum/thread-17842.html?highlight=pyILPER>

3 Prepare the system

Preparing the system – reset the FRAM71B and deactivate FRAM71B modules from memory.

1	Assumed jumpers configuration	
2	Description	Jumper settings
3	<hr/>	
4	Disable SysRAM	[J1: Open] & [J2: Close]
5	Disable E0000 Mapping	[CN2-5: Open]
6	Disable SysRAM Writing	[CN2-4: Open]
7	Enable HPBus Writing	[CN2-3: Open]
8	Enable IRAM Mapping	[CN2-2: Open]
9	Select FRAM Chip	[CN2-1: Open=Bottom_512KB / Close=Top_512KB]

Unmap FRAM71B memory

Remove FRAM71B memory from the memory map and CLAIM previous FREEd ports.

1	POKE "2C000", "00000000000000000000000000000000" [ENTER] -> 32*"0"	
---	--	--

1	[f] [OFF] [ON]	-> Activate the configuration
2	MEM [ENTER]	-> You should have more than 16000 bytes (16.5KB)

Check the default configuration

```
1 SHOW PORT [ENDLINE]
2 0.05 16384 2
3 0      4096 0
4 0.01  4096 0
5 0.02  4096 0
6 0.03  4096 0
```

If there is another setting in the above result it could be that there exist old IRAM etc settings in the FRAM71B. Then you should claim the ports – safest way is:

1. FREE PORT(5.xx) // if it is IRAM already, skip this step
2. CLAIM PORT(5.xx) // kill all contents of that port, and make it empty RAM
3. POKE"2C000", "...00" // POKE two zeroes into the rightmost positions of the config
4. power cycle

If the problems are still present try a total reset – see: <https://www.hpmuseum.org/forum/thread-5044.html>

HP-IL Configuration

Setup HP-IL, ILPer and load FRAM71BTK virtual tape/floppy. Connect all the components:

```
1 HPIL: 71B+IL <=> IL Cables <=> PIL-Box
2 USB: PIL-Box <=> USB Cable <=> PC/Win <=> ILPer or MAC <=> pyILPER
```

ILPer: start and configure software

- Start ILPer.exe software
- Match the "PIL-Box Link" control with the COM port the PIL-Box is using
- Fill the "Mass Storage LIF file" with the LIF image: FRAM71BTK.LIF
- Check the Scope check box to activate IL commands tracing
- Press the Start Button

HP71B: activate interface loop

```
1 [ON] -> You may see some text in ILPer Scope
2 RESTORE IO [ENTER] -> You should see some text in ILPer Scope
```

pyILPER: to check the commands in the terminal window during the installation process
activate tracing in terminal window of pyILPER

```
1 check the Scope -> check box: "Device enabled" and "Show IDY frames Log mode"
```

Now you have to prepare a plan of the modules you want to use and fit them in the available address space. Take care that the addressable banks and the available addresses on the FRAM71B are limited – see picture from FRAM71B configuration in the FRAM71B user manual (p12 to p 14)!!!.

4 A beginners example

This is an easy example from Sylvain Cote. It demonstrates basic bank switching between the Finance (16KB ROM) and the CurveFit (32KB ROM) module and is the best to understand basic configuration.

4.1 Basic Configuration

Connect to pyILPER via PIL-BOX

```

1 POKE "2C000","A3" [ENDLINE] // setup bank No. 1
2                               -> Chip No.0 with FRAM-Block No.3 as 16KB RAM
3 [OFF] [ON]                   -> Activate the configuration
4 MEM [ENDLINE]                -> MEM (32,5KB)

```

	Chip_#	Addr.	Configuration	Description of	LCIM	Type	Size	Port
3	Chip_0	2C000	CONF* E					
4	Chip_0	2C001	F-BLOCK**3	16KB FINANCE ROM	1	ROM	16	5.05
6	Chip_1	2C002	CONF D					
7	Chip_1	2C003	F-BLOCK 4	32KB CURVEFIT ROM	1	ROM	32	5.00

*CONF: Memory configuration nibble value (according to FRAM71B user manual p.14)

**F-Block: 32KB Block in FRAM71B (according to FRAM71B user manual p.13)

4.1.1 Prepare PORT 5 for 16KB Finance ROM

```

1 FREE PORT(5) [ENDLINE] -> create the space to receive the 16KB Finance ROM
2 MEM [ENDLINE]          -> MEM (16.5KB)

4 SHOW PORT [ENDLINE]
5 0.05 16384 2
6 5    16384 1
7 0    4096  0
8 0.01 4096  0
9 0.02 4096  0
10 0.03 4096  0

```

load the FRAMTK LIF image into pyILPER

```

1 COPY ROMCOPY:TAPE [ENDLINE] -> load ROMCOPY LEX file into main memory

```

Prepare for FINANCE module – load the FINANCE LIF image into pyILPER or ILPER

```
1 ROMCOPY FINANCE:TAPE TO :PORT(5) [ENDLINE] -> load FINANCE 16KB ROM into port 5
2 CAT :PORT(5) [ENDLINE] -> Check port 5 Finance ROM content
```

Activating the 16KB Finance ROM in Bank 1 as ROM (Chip No.0 with FRAM-Block No.3)

```
1 POKE "2C000","E3" [ENDLINE] -> activating bank No.1 as ROM
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5) [ENDLINE] -> show port 5 Finance ROM content

5 SHOW PORT [ENDLINE]
6 0.05 16384 2
7 5 16384 2
8 0 4096 0
9 0.01 4096 0
10 0.02 4096 0
11 0.03 4096 0
```

Final validation

```
1 VER$ [ENTER] -> HP71:2CDCC RCPY:E HPIL:1B FIN:A
```

4.1.2 Prepare for CURVEFIT module

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C000","00" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C000","94" [ENDLINE]
2 -> setup bank No.2 Chip No.0 with FRAM-Block No.4 as 32KB RAM

4 [OFF] [ON] -> Activate the configuration
5 CLAIM :PORT(5) [ENDLINE] -> just in case the port was freed by a previous
6 configuration

8 MEM [ENDLINE] -> you should have ~48.5KB of RAM
```

```
1 FREE PORT(5) [ENDLINE] -> create the space to received the 32KB CurveFit ROM
2 MEM [ENDLINE] // you should have ~16.5KB of RAM

4 SHOW PORT [ENDLINE] -> you should see -> Port: 5 / Size: 32768 / Type:1 IRAM
5 0.05 16384 2
6 5 32768 1
7 0 4096 0
8 0.01 4096 0
9 0.02 4096 0
10 0.03 4096 0
```


Prepare for CURVEFIT module –load the CURVEFIT LIF image into pyILPER or ILPER

```
1 ROMCOPY CURVEFIT:TAPE TO :PORT(5) [ENDLINE] -> load CURVEFIT 32KB ROM to port 5
2 CAT :PORT(5) [ENDLINE] -> Check port 5 CurveFit ROM content
```

Activating the 32KB CurveFit ROM in Bank 2 as ROM (Chip No.0 with FRAM-Block No.4)

```
1 POKE "2C000","D4" [ENDLINE] -> activating bank No.1 as ROM
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5) [ENDLINE] // show port 5 Finance ROM content

5 SHOW PORT [ENDLINE]
6 0.05 16384 2
7 5 32768 2
8 0 4096 0
9 0.01 4096 0
10 0.02 4096 0
11 0.03 4096 0
```

Final validation

```
1 VER$ [ENTER] -> HP71:2CDCC RCPY:E HPIL:1B FIT:A
```

4.2 Conventional Bank Switching

Take care of the whole process. Whenever you want to switch between the banks you have to deactivate the actual configuration and activate this step with OFF/ON. Same with activation of the new bank.

4.2.1 Activating the 16KB Finance ROM

Activating the 16KB Finance ROM in Bank 1 as IRAM (Chip No.0 with FRAM-Block No.3)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C000","00" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C000","E3" [ENDLINE] -> activating bank No. 1 as ROM
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5) [ENDLINE] // show port 5 Finance ROM content
```

4.2.2 Activating the 32KB CurveFit ROM

Activating the 32KB CurveFit ROM in Bank 2 as IRAM (Chip No.0 with FRAM-Block No.4)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C000", "00" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C000", "D4" [ENDLINE] // activating bank No.1 as ROM
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5) [ENDLINE] // show port 5 Finance ROM content
```

5 Configuration plan 1 – with 128 KB Main RAM

I chose my most important ROMs and decided to test them with 128 KB Main RAM (in FRAM71B), 32KB IRAM, 41FORTH, JPCROM, MATHROM CURVEFIT, AMPI-STAT, DATA-ACQ, CIRCUIT and FINANCE. Number of Modules are only limited by 15 FRAM71B blocks and the address space. In this example all of the available space is used.

1	POKE "2C000",D3E4D5D69718191A9B9C9D00"								
3	Chip_#	Addr.	Configuration	Description of	LCIM	Type	Size	Port	
4									
5	Chip_0	2C000	CONF* D						
6	Chip_0	2C001	F-BLOCK**3	HC E0000 T41 ROM	1	ROM	32	n/a	
7									
8	Chip_1	2C002	CONF E						
9	Chip_1	2C003	F-BLOCK 4	16KB SC T41 ROM	1	ROM	16	5.00	
10									
11	Chip_2	2C004	CONF D						
12	Chip_2	2C005	F-BLOCK 5	32KB Math ROM	1	ROM	32	5.01	
13									
14	Chip_3	2C006	CONF D						
15	Chip_3	2C007	F-BLOCK 6	32KB JPC ROM	1	ROM	32	5.02	
16									
17	Chip_4	2C008	CONF 9						
18	Chip_4	2C009	F-BLOCK 7	32KB Backup IRAM	1	RAM	32	5.03	
19									
20	Chip_5	2C00A	CONF 1						
21	Chip_5	2C00B	F-BLOCK 8	Main RAM 128KB 1 of 4	0	RAM	32	5.04	
22									
23	Chip_6	2C00C	CONF 1						
24	Chip_6	2C00D	F-BLOCK 9	Main RAM 128KB 2 of 4	0	RAM	32	5.04	
25									
26	Chip_7	2C00E	CONF 1						
27	Chip_7	2C00F	F-BLOCK A	Main RAM 128KB 3 of 4	0	RAM	32	5.04	
28									
29	Chip_8	2C010	CONF 9						
30	Chip_8	2C011	F-BLOCK B	Main RAM 128KB 4 of 4	0	RAM	32	5.04	
31									
32	Chip_9	2C012	CONF D	CURVEFIT					
33	Chip_9	2C013	F-BLOCK C	32 KB Guest ROM	1	RAM	32	5.05	
34									
35	Chip_A	2C014	CONF D	AMPISTAT					
36	Chip_A	2C015	F-BLOCK D	32 KB Guest ROM	1	ROM	32	5.06	
37									

*CONF: Memory configuration nibble value (according to FRAM71B user manual p.14)

**F-Block: 32KB Block in FRAM71B (according to FRAM71B user manual p.13)

Configuration bank switching 1

1	POKE "2C000", "D3E4D5D69718191A9BEEEF00"									
2	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
3										
4	Chip_9	2C012	CONF	E	FINANCE					
5	Chip_9	2C013	F-BLOCK	E	16 KB Guest ROM		1	RAM	16	5.05
6										
7	Chip_A	2C014	CONF	E	CIRCUIT					
8	Chip_A	2C015	F-BLOCK	F	16 KB Guest ROM		1	ROM	16	5.06

Configuration bank switching 2

1	POKE "2C000", "D3E4D5D69718191A9B50D100"									
2	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
3										
4	Chip_9	2C012	CONF	5	Data-ACQ (64KB)					
5	Chip_9	2C013	F-BLOCK	0	32 KB Guest ROM		0	RAM	32	5.05
6										
7	Chip_A	2C014	CONF	D	Data-ACQ (64KB)					
8	Chip_A	2C015	F-BLOCK	1	32 KB Guest ROM		1	ROM	32	5.05
9										

The following guide ist for the 128KB version only. The first part of the configuration is the same for the 96KB version till "Cleaning the ROM testing" section. A whole 96k configuration is in chapter [6](#).

5.1 Start the configuration

1	POKE "2C000", "93A49596979800" [ENTER]		→ Starting setup
2	[f] [OFF] [ON]		→ Activate the configuration
3	MEM [ENTER]		→ You should have around 192KB

CHECK configuration:

1	[SHOWPORT]		
2	0.05	16384	2
3	0	4096	0
4	0.01	4096	0
5	0.02	4096	0
6	0.03	4096	0
7	5	32768	0
8	5.01	16384	0
9	5.02	32768	0
10	5.03	32768	0
11	5.04	32768	0
12	5.05	32768	0

Install FRAM71B ToolKit The following steps will install the FRAM71B ToolKit in IRAM (save area to the configuration in the next steps) who is essential for installing the HP-41 Translator Module.

1	FREE PORT(5.05) [ENTER]	→ Create an IRAM for FRAM71B ToolKit
2	COPY ROMCOPY:TAPE [ENTER]	→ Load the ROMCOPY LEX
3	ROMCOPY FRAMIK:TAPE TO :PORT(5.05) [ENTER]	→ Load FRAM71B ToolKit into IRAM
4	VER\$ [ENTER]	→ HP71:2CDCC RCPY:E HPIL:1B RCPY:E
5	PURGE ROMCOPY [ENTER]	→ Remove ROMCOPY located in main RAM
6	VER\$ [ENTER]	→ HP71:2CDCC HPIL:1B RCPY:E

CHECK configuration:

1	[SHOWPORT]	[RUN MEMBUF]
2		Port Dev Seq Size Addr Type
3	0.05 16384 2	0 0 0 4 78000 0
4	5.05 32768 1	0 1 0 4 7A000 0
5	0 4096 0	0 2 0 4 7C000 0
6	0.01 4096 0	0 3 0 4 7E000 0
7	0.02 4096 0	5 0 0 32 30000 0
8	0.03 4096 0	5 1 0 16 70000 0
9	5 32768 0	5 2 0 32 40000 0
10	5.01 16384 0	5 3 0 32 50000 0
11	5.02 32768 0	5 4 0 32 60000 0
12	5.03 32768 0	0 5 0 16 F0000 2
13	5.04 32768 0	5 5 0 32 E0000 1
15	MEM [ENTER]	→ You should have around 160KB

5.1.1 Edit the configuration on the PC

For comfortable editing in the terminal window of pyILPER on the PC instead fiddling around on the small keyboard of the calculator you can put the prog: PILTERM and KEYBOARD (Lex-File) on the PORT 5.04 (this is the later 32KB IRAM).

```
1 FREE PORT(5.04) [ENTER]          -> Create an IRAM for PILTERM
2 COPY PILTERM:TAPE TO :PORT(5.04)[ENTER]
3 COPY KEYBOARD:TAPE TO :PORT(5.04)[ENTER]
4 [RUN PILTERM]
```

Final validation

```
1 VER$ [ENTER]                    -> HP71:2CDCC HPIL:1B RCPY:E KBD:C
```

Now you can do all operations in the PC-Keyboards

CHECK configuration:

[SHOWPORT]				[RUN MEMBUF]					
				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	68000	0
4	5.04	32768	1	0	1	0	4	6A000	0
5	5.05	32768	1	0	2	0	4	6C000	0
6	0	4096	0	0	3	0	4	6E000	0
7	0.01	4096	0	5	0	0	32	30000	0
8	0.02	4096	0	5	1	0	16	60000	0
9	0.03	4096	0	5	2	0	32	40000	0
10	5	32768	0	5	3	0	32	50000	0
11	5.01	16384	0	5	4	0	32	F0000	2
12	5.02	32768	0	0	5	0	16	E0000	1
13	5.03	32768	0	5	5	0	32	D0000	

Attention!! The addresses and configuration in the next steps are without the above editing possibility in the terminal window. If you want to use it you may recognize a little different results in SHOWPORT and MEMBUF and take care of this in the PEEKs and POKEs.

5.2 Load HC-TRANS41

Load the hidden part of the HP41 Translator ROM. Load HC-TRANS41 image file

```
1 RUN T2R [ENTER]    -> Copy HC Trans41 32KB image to 30000
2                    -> You will see 3FFC0 when the program has ended
```

Remap C0000-CFFFF to E0000-EFFFF

```
1 [ON] [f] [OFF]    -> Shut down the computer
2 Insert Jumper CN2-5 -> Activate Chip_0 E0000 mapping
3 [ON]              -> Wake up the computer
```

Validate E0000-EFFFF content

```
1 PEEK$("E0000",16) [ENTER] -> "0600EF550EDA21EA" validate HC TRANS41 content
2 PEEK$("EFBF0",16) [ENTER] -> "03ED03EE03EF03F0" validate HC TRANS41 content
```

CHECK configuration:

```
1 [SHOWPORT]
2
3 Port Dev Seq Size Addr Type
4 0.05 16384 2 0 0 0 4 68000 0
5 5.04 32768 1 0 1 0 4 6A000 0
6 0 4096 0 0 2 0 4 6C000 0
7 0.01 4096 0 0 3 0 4 6E000 0
8 0.02 4096 0 5 0 0 16 60000 0
9 0.03 4096 0 5 1 0 32 30000 0
10 5 16384 0 5 2 0 32 40000 0
11 5.01 32768 0 5 3 0 32 50000 0
12 5.02 32768 0 0 5 0 16 70000 2
13 5.03 32768 0 5 4 0 32 D0000 1
14 MEM [ENTER] -> You should have around 128KB
```

Reconfigure IIRAM into ROM

```
1 POKE "2C000","D3A49596979800" [ENTER] -> Reconfigure Chip_0
2                               from RAM "(93)A49596979800" to ROM "(D3)A49596979800"
3 [f] [OFF] [ON] -> Activate the configuration
```

Chip_#	Addr.	Configuration	Description	LCIM	Type	Size	Port
Chip_5	2C00A	CONF 9					
Chip_5	2C00B	F-BLOCK 8	32KB FRAM7IBTK IIRAM	1	RAM	32	5.05

New configuration after HC-TRANS41 has been mapped & activated. The action to remap Chip_0 from page 3 to page E has the effect to remove itself from the port assignation. The consequence is that all the others port number has been decreased by .01

5.3 Load SC-TRANS41

Load the visible part of the HP41 Translator ROM. Before Configuration

1	Chip_#	Addr.	Configuration	Description	LCIM	Type	Size	Port
2								
3	Chip_1	2C002	CONF	A				
4	Chip_1	2C003	F-BLOCK 4	16KB SC T41 ROM plan	1	RAM	16	5.00
5								

Load SC-TRANS41 image file

1	FREE PORT(5) [ENTER]	-> Create an IRAM for SC-TRANS41
2	ROMCOPY FTH41ROM:TAPE TO :PORT(5) [ENTER]	-> copy SC-TRANS41 to new IRAM

CHECK configuration:

1	[SHOWPORT]								[RUN MEMBUF]
2				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	60000	0
4	5	16384	1	0	1	0	4	62000	0
5	5.04	32768	1	0	2	0	4	64000	0
6	0	4096	0	0	3	0	4	66000	0
7	0.01	4096	0	5	1	0	32	30000	0
8	0.02	4096	0	5	2	0	32	40000	0
9	0.03	4096	0	5	3	0	32	50000	0
10	5.01	32768	0	0	5	0	16	70000	2
11	5.02	32768	0	5	0	0	16	78000	1
12	5.03	32768	0	5	4	0	32	D0000	1

Remove IRAM identifier

1	POKE "2C000", "D3E49596979800" [ENTER]	> Reconfigure RAM
2		from "D3(A4)9596979800" to ROM "D3(E4)9596979800"
3	[f] [OFF] [ON]	-> Activate the configuration

CHECK configuration:

1	[SHOWPORT]								[RUN MEMBUF]
2				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	60000	0
4	5	16384	2	0	1	0	4	62000	0
5	5.04	32768	1	0	2	0	4	64000	0
6	0	4096	0	0	3	0	4	66000	0
7	0.01	4096	0	5	1	0	32	30000	0
8	0.02	4096	0	5	2	0	32	40000	0
9	0.03	4096	0	5	3	0	32	50000	0
10	5.01	32768	0	0	5	0	16	70000	2
11	5.02	32768	0	5	0	0	16	78000	2
12	5.03	32768	0	5	4	0	32	D0000	1
14	MEM [ENTER]								-> You should have around 111,5KB

Final validation

```

1 VER$ [ENTER]          -> HP71:2CDCC HPIL:1B FTH41:1A EDT:A RCPY:E
2 HP41 [ENTER]          -> ?HP41 EMULATOR 1A? then SIZE ( max. 10000 ) ?
3 31 [ENTER]            -> 0 (the emulator has now 31 data registers)
4 5 3 + [ENTER]         -> 8
5 BYE [ENTER]           -> leave TRANS41 and back to BASIC

```

5.4 Install MATH ROM

The following steps will load the Math ROM

```

1 FREE PORT(5.01) [ENTER]          -> Create an IRAM for MATH ROM
2 COPYMATHROM:TAPE TO :PORT(5.01) [ENTER] -> copy MATH ROM to new IRAM

```

CHECK configuration:

[SHOWPORT]				[RUN MEMBUF]					
				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	50000	0
4	5	16384	2	0	1	0	4	52000	0
5	5.01	32768	1	0	2	0	4	54000	0
6	5.04	32768	1	0	3	0	4	56000	0
7	0	4096	0	5	2	0	32	30000	0
8	0.01	4096	0	5	3	0	32	40000	0
9	0.02	4096	0	0	5	0	16	60000	2
10	0.03	4096	0	5	0	0	16	68000	2
11	5.02	32768	0	5	1	0	32	D0000	1
12	5.03	32768	0	5	4	0	32	C0000	1

Remove IRAM identifier

```

1 PEEK$("D0000",8) [ENTER]          -> "B3DDDDDE" IRAM identifier
2 POKE "D0000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("D0000",8) [ENTER]          -> "00000000" validates the removal of the
4                                     IRAM identifier

```

Reconfigure module type

```

1 POKE "2C000","D3E4D596979800" [ENTER] > Reconfigure RAM
2                                     from "D3E4(95)96979800" to ROM "D3E4(D5)96979800"
3 or short: POKE "2C004","D5"
4 [f] [OFF] [ON]                    -> Activate the configuration
5 RUN MEMBUF [ENTER]                 -> Port Dev Seq Size Addr Type Comment
6                                     -> 5 1 0 32 D0000 2 MATH ROM
7 MEM [ENTER]                        -> You should have around 80KB

```

Final validation

```

1 VER$ [ENTER]          -> HP71:2CDCC HPIL:1B FTH41:1A EDT:A MATH:1A RCPY:E
2 BVAL("1111",2) [ENTER] -> 15

```

Changing original MATHROM Version to version MATH2b7 from J-F Garnier <http://www.jeffcalc.hp41.eu/emu71/mathrom.html#math2>

```
1 POKE "2C004","95" ... config as IRAM in the FRAM71 if it was ROM before
2 [f] [OFF] [ON]                                -> Activate the configuration
3 FREE PORT(5.01)
4 COPY MATH2B7:TAPE TO :PORT(5.01) ... finished if you let it as IRAM

6 POKE "D0000","00000000" ... remove IRAM identifier if configure as ROM
7 POKE "2C004","D5" ... config as ROM
8 [f] [OFF] [ON]                                -> Activate the configuration
```

Final validation

```
1 VER$ [ENTER]                                -> HP71:2CDCC HPIL:1B FTH41:1A EDT:A MATH:2B RCPY:E
2 SEC(30) [ENTER] -> 1.15470053838
```

5.5 Install JPC ROM

The following steps will load the JPC ROM v.F04. Load JPC image file

```
1 FREE PORT(5.02) [ENTER]          -> Create an IRAM for JPC ROM
2 COPY JPCF04:TAPE TO :PORT(5.02) [ENTER] -> copy JPC ROM to new IRAM
```

CHECK configuration:

	[SHOWPORT]					[RUN MEMBUF]						
							Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2				0	0	0	4	40000	0
4	5	16384	2				0	1	0	4	42000	0
5	5.01	32768	2				0	2	0	4	44000	0
6	5.02	32768	1				0	3	0	4	46000	0
7	5.04	32768	1				5	3	0	32	30000	0
8	0	4096	0				0	5	0	16	50000	2
9	0.01	4096	0				5	0	0	16	58000	2
10	0.01	4096	0				5	1	0	32	D0000	2
11	0.03	4096	0				5	2	0	32	C0000	1
12	5.03	32768	0				5	4	0	32	B0000	1

Remove IRAM identifier

```
1 PEEK$("C0000",8) [ENTER]          -> "B3DDDDDE" IRAM identifier
2 POKE "C0000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("C0000",8) [ENTER]          -> "00000000" validates the removal of the
4                                     IRAM identifier
```

Reconfigure module type

```
1 POKE "2C000","D3E4D5D6979800" [ENTER] -> Reconfigure RAM
2                                     from "D3E4D5(96)979800" to ROM "D3E4D5(D6)979800"
3 or short: POKE "2C006","D6"
4 [f] [OFF] [ON]                      -> Activate the configuration
5 RUN MEMBUF [ENTER]                  -> Port Dev Seq Size Addr Type Comment
6                                     -> 5 2 0 32 C0000 2 JPC ROM
7 MEM [ENTER]                         -> You should have around 48KB
```

Final validation

```
1 VER$ [ENTER]          -> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC:F04 HPIL:1B RCPY:E
2 ATH$("123") [ENTER] -> 132333
```

For the 96KB version you can keep 2 * 32KB IRAMs and continue to section "configuration plan 2" on chapter 6.6 if you want.

Changing original MATHROM Version to version MATH2b7 from J-F Garnier <http://www.jeffcalc.hp41.eu/emu71/mathrom.html#math2>

```
1      POKE "2C004","95" ... config as IRAM in the FRAM71 if it was ROM before
2      [f] [OFF] [ON]          -> Activate the configuration
3      FREE PORT(5.01)
4      COPY MATH2B7:TAPE TO :PORT(5.01) ... finished if you let it as IRAM

6      POKE "D0000","00000000" ... remove IRAM identifier if configure as ROM
7      POKE "2C004","D5" ... config as ROM
8      [f] [OFF] [ON]          -> Activate the configuration
9      VER$ ... recognized MATH:2b
10     SEC(30) [ENTER] -> 1.15470053838
```

5.6 Create Backup 32KB IRAM

Allocate a protected memory against Memory Lost for program and data backup

```
1 FREE PORT(5.03) [ENTER] -> Create an IRAM for Backup (Data & Programs)
```

CHECK configuration:

	[SHOWPORT]	[RUN MEMBUF]						
				Port	Dev	Seq	Size	Addr Type
3	0.05	16384	2	0	0	0	4	30000 0
4	5	16384	2	0	1	0	4	32000 0
5	5.01	32768	2	0	2	0	4	34000 0
6	5.02	32768	2	0	3	0	4	36000 0
7	5.03	32768	1	0	5	0	16	40000 2
8	5.04	32768	1	5	0	0	16	48000 2
9	0	4096	0	5	1	0	32	D0000 2
10	0.01	4096	0	5	2	0	32	C0000 2
11	0.02	4096	0	5	3	0	32	B0000 1
12	0.03	4096	0	5	4	0	32	A0000 1
13	MEM [ENTER]	-> You should have around 14KB						

Cleaning the ROM testing section

```
1 COPY ROMCOPY:PORT(5.04) TO :PORT(5.03) [ENTER] -> Needed to load ROM Images
2 COPY MEMBUF:PORT(5.04) TO :PORT(5.03) [ENTER] -> for configure the next ports
3 CLAIM PORT(5.04) [ENTER] -> Integrating the IRAM back into main RAM
4 VER$ [ENTER] -> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC:F04 HPIL:1B RCPY:E
```

CHECK configuration:

	[SHOWPORT]	[RUN MEMBUF]						
				Port	Dev	Seq	Size	Addr Type
3	0.05	16384	2	0	0	0	4	40000 0
4	5	16384	2 FTH41	0	1	0	4	42000 0
5	5.01	32768	2 MATHROM	0	2	0	4	44000 0
6	5.02	32768	2 JPCF04	0	3	0	4	46000 0
7	5.03	32768	1 IRAM	5	4	0	32	30000 0 not allocated
8	0	4096	0	0	5	0	16	50000 2
9	0.01	4096	0	5	0	0	16	58000 2 FTH41
10	0.02	4096	0	5	1	0	32	D0000 2 MATHROM
11	0.02	4096	0	5	2	0	32	C0000 2 JPCF04
12	5.04	32768	0	5	3	0	32	B0000 1 IRAM
13	MEM [ENTER]	-> You should have around 46KB						

5.7 Preparation for "Guest ROMs" and 128KB Main RAM

1	POKE "2C000", "D3E4D5D69798191A9B9C9D00"									
2	[f]	[OFF]	[ON]	-> Activate the configuration						
4	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
5										
6	Chip_9	2C012	CONF	D	CURVEFIT					
7	Chip_9	2C013	F-BLOCK	C	32 KB Guest ROM		1	RAM	32	5.05
8										
9	Chip_A	2C014	CONF	D	AMPISTAT					
10	Chip_A	2C015	F-BLOCK	D	32 KB Guest ROM		1	RAM	32	5.06
11										

CHECK configuration:

1	[SHOWPORT]									
2	[RUN MEMBUF]									
3	0.05	16384	2		Port	Dev	Seq	Size	Addr	Type
4	5	16384	2	FTH41	0	1	0	4	92000	0
5	5.01	32768	2	MATHROM	0	2	0	4	94000	0
6	5.02	32768	2	JPCF04	0	3	0	4	96000	0
7	5.03	32768	1	IRAM	5	4	0	128	30000	0 Main RAM
8	0	4096	0		5	5	0	32	70000	0 not allocated
9	0.01	4096	0		5	6	0	32	80000	0 not allocated
10	0.02	4096	0		0	5	0	16	A0000	2
11	0.02	4096	0		5	0	0	16	A8000	2 FTH41
12	5.04	131072	0	Main RAM	5	1	0	32	D0000	2 MATHROM
13	5.05	32768	0		5	2	0	32	C0000	2 JPCF04
14	5.06	32768	0		5	3	0	32	B0000	1 IRAM
15	MEM [ENTER] → You should have around 207,5KB									

1	VER\$ [ENTER] → HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E									
---	--	--	--	--	--	--	--	--	--	--

5.7.1 Install CURVEFIT and AMPI-STAT

The following steps will load the CURVEFIT and AMPISTAT ROM. Load ROM image files

```

1 FREE PORT(5.05) [ENTER]          -> Create an IRAM for CURVEFIT ROM
2 FREE PORT(5.06) [ENTER]          -> Create an IRAM for AMPI-STAT ROM
3 ROMCOPY CURVEFIT:TAPE TO :PORT(5.05) [ENTER] -> copy CURVEFIT to new IRAM
4 ROMCOPY AMPISTAT:TAPE TO :PORT(5.06) [ENTER] -> copy AMPISTAT to new IRAM

```

CHECK configuration:

```

1 [SHOWPORT]
2
3 Port Dev Seq Size Addr Type
4 0.05 16384 2 FTH41 0 0 0 4 70000 0
5 5 16384 2 MATHROM 0 1 0 4 72000 0
6 5.01 32768 2 JPCF04 0 2 0 4 74000 0
7 5.02 32768 2 JPCF04 0 3 0 4 76000 0
8 5.03 32768 1 IRAM 5 4 0 128 30000 0 Main RAM
9 5.05 32768 1 CURVEFIT 0 5 0 16 80000 2
10 5.06 32768 1 AMPISTAT 5 0 0 16 88000 2 FTH41
11 0 4096 0 5 1 0 32 D0000 2 MATHROM
12 0.01 4096 0 5 2 0 32 C0000 2 JPCF04
13 0.02 4096 0 5 3 0 32 B0000 1 IRAM
14 0.03 4096 0 5 5 0 32 A0000 1 CURVEFIT
15 5.04 131072 0 Main RAM 5 6 0 32 90000 1 AMPISTAT
MEM [ENTER] -> You should have around 144 KB

```

Remove IRAM identifier

```

1 PEEK$("A0000",8) [ENTER] -> "B3DDDDDE" IRAM identifier CURVEFIT
2 POKE "A0000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("A0000",8) [ENTER] -> "00000000" validates the removal
4 of the IRAM identifier

6 PEEK$("90000",8) [ENTER] -> "B3DDDDDE" IRAM identifier AMPISTAT
7 POKE "90000","00000000" [ENTER] -> Remove the IRAM identifier
8 PEEK$("90000",8) [ENTER] -> "00000000" validates the removal
9 of the IRAM identifier

```

Reconfigure module type for both ROM modules

```

1 POKE "2C000","D3E4D5D69718191A9BDCDD00" [ENTER] -> Reconfigure RAM
2 from D3E4D5D69718191A9B(9C)(9D)00" to ROM "D3E4D5D69718191A9B(DC)(DD)00"
3 or short: POKE "2C012","DCDD00"
4 [f] [OFF] [ON] -> Activate the configuration

```

Final validation

1	VER\$ [ENTER] —> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E
2	FIT:A AMPISTAT:A
3	RUN CFIT [ENTER] —> Data Edit Fit Quit?
4	RUN AMPISTAT [ENTER] —> Data Edit Menu Quit?

5.8 Preparation for FINANCE and CIRCUIT modul in Bank 1

1	Chip_#	Addr.	Configuration	Description	of	LCIM	Type	Size	Port
2									
3	Chip_9	2C012	CONF E	FINANCE					
4	Chip_9	2C013	F-BLOCK E	16 KB Guest ROM		1	RAM	16	5.05
5									
6	Chip_A	2C014	CONF E	CIRCUIT					
7	Chip_A	2C015	F-BLOCK F	16 KB Guest ROM		1	ROM	16	5.06
8									

First deactivate the "Guest ROM" before switching to Bank 1 for the new ROM modules.

```

1 POKE "2C000", "D3E4D5D69718191A9B000000" [ENTER] -> prevent a computer freeze
2                                     and/or a memory lost
3 or short POKE "2C012", "000000"
4 [f] [OFF] [ON] -> Activate the configuration

```

Bank switching to Bank No 1

```

1 POKE "2C000", "D3E4D5D69718191A9BAEAF00" -> prepare as RAM
2 or short POKE "2C012", "AEAF"
3 [f] [OFF] [ON] -> Activate the configuration

```

5.8.1 Install FINANCE and CIRCUIT

The following steps will load the FINANCE and CIRCUIT ROM Load ROM image file

```

1 FREE PORT(5.05) [ENTER] -> Create an IRAM for FINANCE ROM
2 FREE PORT(5.06) [ENTER] -> Create an IRAM for CIRCUIT ROM
3 ROMCOPY FINANCE:TAPE TO :PORT(5.05) [ENTER] -> copy FINANCE to new IRAM
4 ROMCOPY CIRCUIT:TAPE TO :PORT(5.06) [ENTER] -> copy CIRCUIT to new IRAM

```

CHECK configuration:

```

1 [SHOWPORT] [RUN MEMBUF]
2
3 Port Dev Seq Size Addr Type
4 0.05 16384 2 0 0 0 4 70000 0
5 5 16384 2 FTH41 0 1 0 4 72000 0
6 5.01 32768 2 MATHROM 0 2 0 4 74000 0
7 5.02 32768 2 JPCF04 0 3 0 4 76000 0
8 5.03 32768 1 IRAM 5 4 0 128 30000 0 Main RAM
9 5.05 32768 1 FINANCE 0 5 0 16 80000 2
10 5.06 32768 1 CIRCUIT 5 0 0 16 88000 2 FTH41
11 0 4096 0 5 1 0 32 D0000 2 MATHROM
12 0.01 4096 0 5 2 0 32 C0000 2 JPCF04
13 0.02 4096 0 5 3 0 32 B0000 1 IRAM
14 0.03 4096 0 5 5 0 16 90000 1 FINANCE
15 5.04 131072 0 Main RAM 5 6 0 16 98000 1 CIRCUIT
MEM [ENTER] -> You should have around 143,5KB

```

Remove IRAM identifier

```
1 PEEK$("90000",8) [ENTER]      -> "B3DDDDDE" IRAM identifier
2 POKE "90000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("90000",8) [ENTER]      -> "00000000" validates the removal of the
4                               IRAM identifier

6 PEEK$("98000",8) [ENTER]      -> "B3DDDDDE" IRAM identifier
7 POKE "98000","00000000" [ENTER] -> Remove the IRAM identifier
8 PEEK$("98000",8) [ENTER]      -> "00000000" validates the removal of the
9                               IRAM identifier
```

Reconfigure module type

```
1 POKE "2C000","D3E4D5D69718191A9BEEEEF00" [ENTER] -> Reconfigure RAM
2           from "D3E4D5D69718191A9B(AEAF)00" to ROM "D3E4D5D69718191A9B(EEEEF)00"
3 or short POKE "2C012","EEEEF00"
4 [ f ] [OFF] [ON]                -> Activate the configuration
```

Final validation

```
1 VER$ [ENTER]  -> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E
2               FIN:A CIRC:A
3 RUN TVM [ENTER] -> For help, press H :
4 RUN CNAP [ENTER] -> MAXIMUM NODES = 49 -> Nw Ad D1 Ch Pr F1 0 ?
```

5.9 Preparation for DATA-ACQ modul in Bank 2

1	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
2										
3	Chip_9	2C012	CONF	5	Data-ACQ (64KB)					
4	Chip_9	2C013	F-BLOCK	0	32 KB Guest ROM		0	RAM	32	5.05
5										
6	Chip_A	2C014	CONF	D	Data-ACQ (64KB)					
7	Chip_A	2C015	F-BLOCK	1	32 KB Guest ROM		1	ROM	32	5.05
8										

For detailed installation read section [6.8.2](#)

5.10 Conventional Bank Switching

Take care of the whole process. Whenever you want to switch between the banks you have to deactivate the actual configuration and activate this step with OFF/ON. Same with activation of the new bank.

5.10.1 Activating the 16KB FINANCE and CIRCUIT ROM

Activating the 16KB Finance ROM in Bank 1 as IRAM (Chip No.0 with FRAM-Block No.3)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C0012","000000" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C012","EEEF00" [ENDLINE] -> activating bank No. 1 as ROM
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5.05) [ENDLINE] // show port 5 FINANCE ROM content
```

5.10.2 Activating the 32KB CURVEFIT and AMPISTAT ROM

Activating the 32KB CurveFit ROM in Bank 2 as IRAM (Chip No.0 with FRAM-Block No.4)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C012","000000" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C012","DCDD00" [ENDLINE] // activating bank No.1 as ROM
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5.05) [ENDLINE] // show port 5 CURVEFIT ROM content
```

6 Configuration plan 2 – with 96 KB Main RAM

I choose my main used ROMs and decided to test them with 96 KB Main RAM, 2 * 32KB IRAM (i.e. for testing purposes of other ROM modules or more backup space) , 41FORTH, JPCROM, MATHROM CURVEFIT, AMPISTAT, DATA-ACQ, CIRCUIT (or TEXT-EDITOR) and FINANCE. Number of Modules are only limited by 15 FRAM71B blocks and the address space.

1	POKE "2C000",D3E4D5D69798191A9B9DCD00"							
3	Chip_#	Addr.	Configuration	Description of	LCIM	Type	Size	Port
4								
5	Chip_0	2C000	CONF* D					
6	Chip_0	2C001	F-BLOCK**3	HC E0000 T41 ROM	1	ROM	32	n/a
7								
8	Chip_1	2C002	CONF E					
9	Chip_1	2C003	F-BLOCK 4	16KB SC T41 ROM	1	ROM	16	5.00
10								
11	Chip_2	2C004	CONF D					
12	Chip_2	2C005	F-BLOCK 5	32KB Math ROM	1	ROM	32	5.01
13								
14	Chip_3	2C006	CONF D					
15	Chip_3	2C007	F-BLOCK 6	32KB JPC ROM	1	ROM	32	5.02
16								
17	Chip_4	2C008	CONF 9					
18	Chip_4	2C009	F-BLOCK 7	32KB Backup IRAM	1	RAM	32	5.03
19								
20	Chip_5	2C00A	CONF 9					
21	Chip_5	2C00B	F-BLOCK 8	32KB Test IRAM	1	RAM	32	5.04
22								
23	Chip_6	2C00C	CONF 1					
24	Chip_6	2C00D	F-BLOCK 9	Main RAM 96KB 1 of 3	0	RAM	32	5.05
25								
26	Chip_7	2C00E	CONF 1					
27	Chip_7	2C00F	F-BLOCK A	Main RAM 96KB 2 of 3	0	RAM	32	5.05
28								
29	Chip_8	2C010	CONF 9					
30	Chip_8	2C011	F-BLOCK B	Main RAM 96KB 3 of 3	0	RAM	32	5.05
31								
32	Chip_9	2C012	CONF D	CURVEFIT				
33	Chip_9	2C013	F-BLOCK C	32 KB Guest ROM	1	RAM	32	5.06
34								
35	Chip_A	2C014	CONF D	AMPISTAT				
36	Chip_A	2C015	F-BLOCK D	32 KB Guest ROM	1	ROM	32	5.07
37								

*CONF: Memory configuration nibble value (according to FRAM71B user manual p.14)

**F-Block: 32KB Block in FRAM71B (according to FRAM71B user manual p.13)

Configuration bank switching 1

1	POKE "2C000", "D3E4D5D69718191A9BEEEF00"									
2	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
3										
4	Chip_9	2C012	CONF	E	FINANCE					
5	Chip_9	2C013	F-BLOCK	E	16 KB Guest ROM		1	RAM	16	5.06
6										
7	Chip_A	2C014	CONF	E	CIRCUIT					
8	Chip_A	2C015	F-BLOCK	F	16 KB Guest ROM		1	ROM	16	5.07

Configuration bank switching 2

1	POKE "2C000", "D3E4D5D69718191A9B50D100"									
2	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
3										
4	Chip_9	2C012	CONF	5	Data-ACQ (64KB)					
5	Chip_9	2C013	F-BLOCK	0	32 KB Guest ROM		0	RAM	32	5.06
6										
7	Chip_A	2C014	CONF	D	Data-ACQ (64KB)					
8	Chip_A	2C015	F-BLOCK	1	32 KB Guest ROM		1	ROM	32	5.06
9										

6.1 Start the configuration

1	POKE "2C000", "93A49596979800" [ENTER] → Starting setup									
2	[f] [OFF] [ON] → Activate the configuration									
3	MEM [ENTER] → You should have around 192KB									

CHECK configuration:

1	[SHOWPORT]									
2	0.05	16384	2							
3	0	4096	0							
4	0.01	4096	0							
5	0.02	4096	0							
6	0.03	4096	0							
7	5	32768	0							
8	5.01	16384	0							
9	5.02	32768	0							
10	5.03	32768	0							
11	5.04	32768	0							
12	5.05	32768	0							

If this differs and you made some configuration experiments before you should CLAIM the PORTs.

Install FRAM71B ToolKit The following steps will install the FRAM71B ToolKit who is essential for installing the HP-41 Translator Module.

1	FREE PORT(5.05) [ENTER]	→ Create an IRAM for FRAM71B ToolKit
2	COPY ROMCOPY:TAPE [ENTER]	→ Load the ROMCOPY LEX
3	ROMCOPY FRAMIK:TAPE TO :PORT(5.05) [ENTER]	→ Load FRAM71B ToolKit into IRAM
4	VER\$ [ENTER]	→ HP71:2CDCC RCPY:E HPIL:1B RCPY:E
5	PURGE ROMCOPY [ENTER]	→ Remove ROMCPY located in main RAM
6	VER\$ [ENTER]	→ HP71:2CDCC HPIL:1B RCPY:E

For comfortable editing in the terminal window of pyILPER on the PC instead fiddling around on the small keyboard of the calculator you can put the prog: PILTERM and KEYBOARD (Lex-File) on the PORT 5.05

1	COPY PILTERM2:TAPE TO :PORT(5.05) [ENTER]
2	COPY KEYBOARD:TAPE TO :PORT(5.05) [ENTER]
3	[RUN PILTERM2]

Now you can do all operations in the PC-Keybord

CHECK configuration:

1	[SHOWPORT]	[RUN MEMBUF]
2		Port Dev Seq Size Addr Type
3	0.05 16384 2	0 0 0 4 78000 0
4	5.05 32768 1	0 1 0 4 7A000 0
5	0 4096 0	0 2 0 4 7C000 0
6	0.01 4096 0	0 3 0 4 7E000 0
7	0.02 4096 0	5 0 0 32 30000 0
8	0.03 4096 0	5 1 0 16 70000 0
9	5 32768 0	5 2 0 32 40000 0
10	5.01 16384 0	5 3 0 32 50000 0
11	5.02 32768 0	5 4 0 32 60000 0
12	5.03 32768 0	0 5 0 16 F0000 2
13	5.04 32768 0	5 5 0 32 E0000 1
15	MEM [ENTER]	→ You should have around 160KB

6.2 Load HC-TRANS41

Load the hidden part of the HP41 Translator ROM. Load HC-TRANS41 image file

```
1 RUN T2R [ENTER]    -> Copy HC Trans41 32KB image to 30000
2                    -> You will see 3FFC0 when the program has ended
```

Remap C0000-CFFFF to E0000-EFFFF

```
1 [ON] [f] [OFF]    -> Shut down the computer
2 Insert Jumper CN2-5 -> Activate Chip_0 E0000 mapping
3 [ON]              -> Wake up the computer
```

Validate E0000-EFFFF content

```
1 PEEK$("E0000",16) [ENTER] -> "0600EF550EDA21EA" validate HC TRANS41 content
2 PEEK$("EFBF0",16) [ENTER] -> "03ED03EE03EF03F0" validate HC TRANS41 content
```

CHECK configuration:

```
1 [SHOWPORT]
2
3 Port Dev Seq Size Addr Type
4 0.05 16384 2 0 0 0 4 68000 0
5 5.04 32768 1 0 1 0 4 6A000 0
6 0 4096 0 0 2 0 4 6C000 0
7 0.01 4096 0 0 3 0 4 6E000 0
8 0.02 4096 0 5 0 0 16 60000 0
9 0.03 4096 0 5 1 0 32 30000 0
10 5 16384 0 5 2 0 32 40000 0
11 5.01 32768 0 5 3 0 32 50000 0
12 5.02 32768 0 0 5 0 16 70000 2
13 5.03 32768 0 5 4 0 32 D0000 1
14 MEM [ENTER] -> You should have around 128KB
```

Reconfigure IIRAM into ROM

```
1 POKE "2C000","D3A49596979800" [ENTER] -> Reconfigure Chip_0
2                                from RAM "(93)A49596979800" to ROM "(D3)A49596979800"
3 [f] [OFF] [ON] -> Activate the configuration
```

Chip_#	Addr.	Configuration	Description	LCIM	Type	Size	Port
Chip_5	2C00A	CONF 9					
Chip_5	2C00B	F-BLOCK 8	32KB FRAM7IBTK IIRAM	1	RAM	32	5.05

New configuration after HC-TRANS41 has been mapped & activated. The action to remap Chip_0 from page 3 to page E has the effect to remove itself from the port assignation. The consequence is that all the others port number has been decreased by .01

6.3 Load SC-TRANS41

Load the visible part of the HP41 Translator ROM. Before Configuration

1	Chip_#	Addr.	Configuration	Description	LCIM	Type	Size	Port
2								
3	Chip_1	2C002	CONF	A				
4	Chip_1	2C003	F-BLOCK 4	16KB SC T41 ROM plan	1	RAM	16	5.00
5								

Load SC-TRANS41 image file

1	FREE PORT(5) [ENTER]	→ Create an IRAM for SC-TRANS41
2	ROMCOPY FTH41ROM:TAPE TO :PORT(5) [ENTER]	→ copy SC-TRANS41 to new IRAM

CHECK configuration:

1	[SHOWPORT]								[RUN MEMBUF]
2				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	60000	0
4	5	16384	1	0	1	0	4	62000	0
5	5.04	32768	1	0	2	0	4	64000	0
6	0	4096	0	0	3	0	4	66000	0
7	0.01	4096	0	5	1	0	32	30000	0
8	0.02	4096	0	5	2	0	32	40000	0
9	0.03	4096	0	5	3	0	32	50000	0
10	5.01	32768	0	0	5	0	16	70000	2
11	5.02	32768	0	5	0	0	16	78000	1
12	5.03	32768	0	5	4	0	32	D0000	1

Remove IRAM identifier

1	POKE "2C000", "D3E49596979800" [ENTER]	> Reconfigure RAM
2		from "D3(A4)9596979800" to ROM "D3(E4)9596979800"
3	[f] [OFF] [ON]	→ Activate the configuration

CHECK configuration:

1	[SHOWPORT]								[RUN MEMBUF]
2				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	60000	0
4	5	16384	2	0	1	0	4	62000	0
5	5.04	32768	1	0	2	0	4	64000	0
6	0	4096	0	0	3	0	4	66000	0
7	0.01	4096	0	5	1	0	32	30000	0
8	0.02	4096	0	5	2	0	32	40000	0
9	0.03	4096	0	5	3	0	32	50000	0
10	5.01	32768	0	0	5	0	16	70000	2
11	5.02	32768	0	5	0	0	16	78000	2
12	5.03	32768	0	5	4	0	32	D0000	1
14	MEM [ENTER]								→ You should have around 111,5KB

Final validation

```

1 VER$ [ENTER]          -> HP71:2CDC HPIL:1B FTH41:1A EDT:A RCPY:E
2 HP41 [ENTER]          -> ?HP41 EMULATOR 1A? then SIZE ( max. 10000 ) ?
3 31 [ENTER]            -> 0 (the emulator has now 31 data registers)
4 5 3 + [ENTER]         -> 8
5 BYE [ENTER]           -> leave TRANS41 and back to BASIC
6 PURGE FTH41RAM -> to free the RAM

```

6.4 Install MATH ROM

The following steps will load the Math ROM

```

1 FREE PORT(5.01) [ENTER]          -> Create an IRAM for MATH ROM
2 COPYMATHROM:TAPE TO :PORT(5.01) [ENTER] -> copy MATH ROM to new IRAM

```

CHECK configuration:

[SHOWPORT]			[RUN MEMBUF]					
			Port	Dev	Seq	Size	Addr	Type
3	0.05	16384 2	0	0	0	4	50000	0
4	5	16384 2	0	1	0	4	52000	0
5	5.01	32768 1	0	2	0	4	54000	0
6	5.04	32768 1	0	3	0	4	56000	0
7	0	4096 0	5	2	0	32	30000	0
8	0.01	4096 0	5	3	0	32	40000	0
9	0.02	4096 0	0	5	0	16	60000	2
10	0.03	4096 0	5	0	0	16	68000	2
11	5.02	32768 0	5	1	0	32	D0000	1
12	5.03	32768 0	5	4	0	32	C0000	1

Remove IRAM identifier

```

1 PEEK$("D0000",8) [ENTER]          -> "B3DDDDDE" IRAM identifier
2 POKE "D0000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("C0000",8) [ENTER]          -> "00000000" validates the removal of the
4                                     IRAM identifier

```

Reconfigure module type

```

1 POKE "2C000","D3E4D596979800" [ENTER] > Reconfigure RAM
2                                     from "D3E4(95)96979800" to ROM "D3E4(D5)96979800"
3 or short: POKE "2C004","D5"
4 [f] [OFF] [ON]                    -> Activate the configuration
5 RUN MEMBUF [ENTER]                 -> Port Dev Seq Size Addr Type Comment
6                                     -> 5 1 0 32 D0000 2 MATH ROM
7 MEM [ENTER]                        -> You should have around 80KB

```

Final validation

```
1 VER$ [ENTER]      -> HP71:2CDCC HPIL:1B FTH41:1A EDT:A MATH:1A RCPY:E
2 BVAL("1111",2) [ENTER] -> 15
```

Changing original MATHROM Version to version MATH2b7 from J-F Garnier <http://www.jeffcalc.hp41.eu/emu71/mathrom.html#math2>

```
1 POKE "2C004","95" ... config as IRAM in the FRAM71 if it was ROM before
2 [f] [OFF] [ON]                                     -> Activate the configuration
3 FREE PORT(5.01)
4 COPY MATH2B7:TAPE TO :PORT(5.01) ... finished if you let it as IRAM

6 POKE "D0000","00000000" ... remove IRAM identifier if configure as ROM
7 POKE "2C004","D5" ... config as ROM
8 [f] [OFF] [ON]                                     -> Activate the configuration
```

Final validation

```
1 VER$ [ENTER]      -> HP71:2CDCC HPIL:1B FTH41:1A EDT:A MATH:2B RCPY:E
2 SEC(30) [ENTER] -> 1.15470053838
```

6.5 Install JPC ROM

The following steps will load the JPC ROM v.F04. Load JPC image file

```
1 FREE PORT(5.02) [ENTER]          -> Create an IRAM for JPC ROM
2 COPY JPCF04:TAPE TO :PORT(5.02) [ENTER] -> copy JPC ROM to new IRAM
```

CHECK configuration:

[SHOWPORT]				[RUN MEMBUF]					
				Port	Dev	Seq	Size	Addr	Type
3	0.05	16384	2	0	0	0	4	40000	0
4	5	16384	2	0	1	0	4	42000	0
5	5.01	32768	2	0	2	0	4	44000	0
6	5.02	32768	1	0	3	0	4	46000	0
7	5.04	32768	1	5	3	0	32	30000	0
8	0	4096	0	0	5	0	16	50000	2
9	0.01	4096	0	5	0	0	16	58000	2
10	0.01	4096	0	5	1	0	32	D0000	2
11	0.03	4096	0	5	2	0	32	C0000	1
12	5.03	32768	0	5	4	0	32	B0000	1

Remove IRAM identifier

```
1 PEEK$("C0000",8) [ENTER]          -> "B3DDDDDE" IRAM identifier
2 POKE "C0000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("C0000",8) [ENTER]          -> "00000000" validates the removal of the
4                                     IRAM identifier
```

Reconfigure module type

```
1 POKE "2C000","D3E4D5D6979800" [ENTER] -> Reconfigure RAM
2                                     from "D3E4D5(96)979800" to ROM "D3E4D5(D6)979800"
3 or short: POKE "2C006","D6"
4 [f] [OFF] [ON]                    -> Activate the configuration
5 RUN MEMBUF [ENTER]                -> Port Dev Seq Size Addr Type Comment
6                                     -> 5 2 0 32 C0000 2 JPC ROM
7 MEM [ENTER]                       -> You should have around 48KB
```

Final validation

```
1 VER$ [ENTER]                    -> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC:F04 HPIL:1B RCPY:E
2 ATH$("123") [ENTER]             -> 132333
```

6.6 Create Backup 32KB + 32KB Test IRAM

Allocate a protected memory against Memory Lost for program and data backup. Let both spaces for IRAM.

1	FREE PORT(5.03) [ENTER] → Create an IRAM									
	CHECK configuration:									
1	[SHOWPORT]			[RUN MEMBUF]						
2				Port	Dev	Seq	Size	Addr	Type	
3	0.05	16384	2	0	0	0	4	30000	0	
4	5	16384	2 FTH41	0	1	0	4	32000	0	
5	5.01	32768	2 MATHROM	0	2	0	4	34000	0	
6	5.02	32768	2 JPCF04	0	3	0	4	36000	0	
7	5.03	32768	1 IRAM 1	0	5	0	16	40000	2	
8	5.04	32768	1 IRAM 2	5	0	0	16	48000	2 FTH41	
9	0	4096	0	5	1	0	32	D0000	2 MATHROM	
10	0.01	4096	0	5	2	0	32	C0000	2 JPCF04	
11	0.02	4096	0	5	3	0	32	B0000	1 IRAM 1	
12	5.03	4096	0	5	4	0	32	A0000	1 IRAM 2	
13	MEM [ENTER]			→ You should have around 16KB						

6.7 Preparation for "Guest ROMs" and 96KB Main RAM

1	POKE "2C000", "D3E4D5D69798191A9B9C9D00"									
2	[f]	[OFF]	[ON]	-> Activate the configuration						
4	Chip_#	Addr.	Configuration		Description	of	LCIM	Type	Size	Port
5										
6	Chip_9	2C012	CONF	9	CURVEFIT					
7	Chip_9	2C013	F-BLOCK	C	32 KB Guest ROM		1	RAM	32	5.06
8										
9	Chip_A	2C014	CONF	9	AMPISTAT					
10	Chip_A	2C015	F-BLOCK	D	32 KB Guest ROM		1	ROM	32	5.07
11										

CHECK configuration:

1	[SHOWPORT]									
2	[RUN MEMBUF]									
				Port	Dev	Seq	Size	Addr	Type	
3	0.05	16384	2	0	0	0	4	80000	0	
4	5	16384	2 FTH41	0	1	0	4	82000	0	
5	5.01	32768	2 MATHROM	0	2	0	4	84000	0	
6	5.02	32768	2 JPCF04	0	3	0	4	86000	0	
7	5.03	32768	1 IRAM 1	5	5	0	96	30000	0	Main RAM
8	5.04	32768	1 IRAM 2	5	6	0	32	60000	0	CURVEFIT
9	0	4096	0	5	7	0	32	70000	0	AMPISTAT
10	0.01	4096	0	0	5	0	16	90000	2	
11	0.02	4096	0	5	0	0	16	98000	2	FTH41
12	0.03	4096	0	5	1	0	32	D0000	2	MATHROM
13	5.05	98304	0 Main RAM	5	2	0	32	C0000	2	JPCF04
14	5.06	32768	2 CURVEFIT	5	3	0	32	B0000	2	IRAM 1
15	5.07	32768	2 AMPISTAT	5	4	0	32	A0000	2	IRAM 2
17	MEM [ENTER] → You should have around 176KB									

1	VER\$ [ENTER] → HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E									
---	--	--	--	--	--	--	--	--	--	--

6.7.1 Install CURVEFIT and AMPI-STAT

The following steps will load the CURVEFIT and AMPISTAT ROM. Load ROM image files

```

1 FREE PORT(5.06) [ENTER]          -> Create an IRAM for CURVEFIT ROM
2 FREE PORT(5.07) [ENTER]          -> Create an IRAM for AMPI-STAT ROM
3 ROMCOPY CURVEFIT:TAPE TO :PORT(5.06) [ENTER] -> copy CURVEFIT to new IRAM
4 ROMCOPY AMPISTAT:TAPE TO :PORT(5.07) [ENTER] -> copy AMPISTAT to new IRAM

```

CHECK configuration:

```

1 [SHOWPORT]
2
3 Port Dev Seq Size Addr Type
4 0.05 16384 2 0 0 0 4 60000 0
5 5 16384 2 FTH41 0 1 0 4 62000 0
6 5.01 32768 2 MATHROM 0 2 0 4 64000 0
7 5.02 32768 2 JPCF04 0 3 0 4 66000 0
8 5.03 32768 1 IRAM 1 5 5 0 96 30000 0 Main RAM
9 5.04 32768 1 IRAM 2 0 5 0 16 70000 2
10 5.06 32768 1 CURVEFIT 5 0 0 16 78000 2 FTH41
11 5.07 32768 1 AMPISTAT 5 1 0 32 D0000 2 MATHROM
12 0 4096 0 5 2 0 32 C0000 2 JPCF04
13 0.01 4096 0 5 3 0 32 B0000 1 IRAM 1
14 0.02 4096 0 5 4 0 32 A0000 1 IRAM 2
15 0.03 4096 0 5 6 0 32 90000 1 CURVEFIT
16 5.05 98304 0 Main RAM 5 7 0 32 80000 1 AMPISTAT
MEM [ENTER] -> You should have around 112 KB

```

Remove IRAM identifier

```

1 PEEK$("90000",8) [ENTER] -> "B3DDDDDE" IRAM identifier
2 POKE "90000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("90000",8) [ENTER] -> "00000000" validates the removal
4 of the IRAM identifier
6 PEEK$("80000",8) [ENTER] -> "B3DDDDDE" IRAM identifier
7 POKE "80000","00000000" [ENTER] -> Remove the IRAM identifier
8 PEEK$("80000",8) [ENTER] -> "00000000" validates the removal
9 of the IRAM identifier

```

Reconfigure module type

```

1 POKE "2C000","D3E4D5D69798191A9BDCDD00" [ENTER] -> Reconfigure RAM
2 from "D3E4D5D69798191A9B(9C9D)00" to ROM "D3E4D5D69798191A9B(DCDD)00"
3 or short_ POKE "2C012","DCDD00"
4 [f] [OFF] [ON] -> Activate the configuration

```

Final validation

1	VER\$ [ENTER] —> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E
2	FIT:A AMPISTAT:A
3	RUN CFIT [ENTER] —> Data Edit Fit Quit?
4	RUN AMPISTAT [ENTER] —> Data Edit Menu Quit?

6.8 Preparation for FINANCE and CIRCUIT modul in Bank 1

1	Chip_#	Addr.	Configuration	Description	of	LCIM	Type	Size	Port
2									
3	Chip_9	2C012	CONF E	FINANCE					
4	Chip_9	2C013	F-BLOCK E	16 KB Guest ROM		1	RAM	16	5.06
5									
6	Chip_A	2C014	CONF E	CIRCUIT					
7	Chip_A	2C015	F-BLOCK F	16 KB Guest ROM		1	ROM	16	5.07
8									

First deactivate the "Guest ROM" before switching to Bank 1 for the new ROM modules.

```

1 POKE "2C000", "D3E4D5D69798191A9B000000" [ENTER] -> prevent a computer freeze
2                                     and/or a memory lost
3 or short POKE "2C012", "000000"
4 [f] [OFF] [ON] -> Activate the configuration

```

Bank switching to Bank No 1

```

1 POKE "2C000", "D3E4D5D69798191A9BAEAF00" -> prepare as RAM
2 or short POKE "2C012", "AEAF00"
3 [f] [OFF] [ON] -> Activate the configuration

```

6.8.1 Install FINANCE and CIRCUIT

The following steps will load the FINANCE and CIRCUIT ROM Load ROM image file

```

1 FREE PORT(5.06) [ENTER] -> Create an IRAM for FINANCE ROM
2 FREE PORT(5.07) [ENTER] -> Create an IRAM for CIRCUIT ROM
3 ROMCOPY FINANCE:TAPE TO :PORT(5.06) [ENTER] -> copy FINANCE to new IRAM
4 ROMCOPY CIRCUIT:TAPE TO :PORT(5.07) [ENTER] -> copy CIRCUIT to new IRAM

```

CHECK configuration:

```

1 [[SHOWPORT] [RUN MEMBUF]
2
3 0.05 16384 2 0 0 0 4 60000 0
4 5 16384 2 FTH41 0 1 0 4 62000 0
5 5.01 32768 2 MATHROM 0 2 0 4 64000 0
6 5.02 32768 2 JPCF04 0 3 0 4 66000 0
7 5.03 32768 1 IRAM 1 5 5 0 96 30000 0 Main RAM
8 5.04 32768 1 IRAM 2 0 5 0 16 70000 2
9 5.06 16384 1 FINANCE 5 0 0 16 78000 2 FTH41
10 5.07 16384 1 CIRCUIT 5 1 0 32 D0000 2 MATHROM
11 0 4096 0 5 2 0 32 C0000 2 JPCF04
12 0.01 4096 0 5 3 0 32 B0000 1 IRAM 1
13 0.02 4096 0 5 4 0 32 A0000 1 IRAM 2
14 0.03 4096 0 5 6 0 16 80000 1 FINANCE
15 5.05 98304 0 Main RAM 5 7 0 16 88000 1 CIRCUIT
16 MEM [ENTER] -> You should have around 112 KB

```

Remove IRAM identifier

```

1 PEEK$("80000",8) [ENTER]      -> "B3DDDDDE" IRAM identifier
2 POKE "80000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("80000",8) [ENTER]      -> "00000000" validates the removal of the
4                               IRAM identifier

6 PEEK$("88000",8) [ENTER]      -> "B3DDDDDE" IRAM identifier
7 POKE "88000","00000000" [ENTER] -> Remove the IRAM identifier
8 PEEK$("88000",8) [ENTER]      -> "00000000" validates the removal of the
9                               IRAM identifier

```

Reconfigure module type

```

1 POKE "2C000","D3E4D5D69798191A9BEEEEF00" [ENTER] -> Reconfigure RAM
2           from "D3E4D5D69798191A9B(AEAF)00" to ROM "D3E4D5D69798191A9B(EEEEF)00"
3 or short POKE "2C012","EEEEF00"
4 [ f ] [OFF] [ON]                -> Activate the configuration

```

Final validation

```

1 VER$ [ENTER]  -> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E
2               FIN:A CIRC:A
3 RUN TVM [ENTER] -> For help, press H :
4 RUN CNAP [ENTER] -> MAXIMUM NODES = 49 -> Nw Ad D1 Ch Pr F1 0 ?

```

6.8.2 Install DATA-ACQ

1	Chip_#	Addr.	Configuration	Description	of	LCIM	Type	Size	Port
2									
3	Chip_9	2C012	CONF 5	Data-ACQ (64KB)					
4	Chip_9	2C013	F-BLOCK 0	32 KB Guest ROM		0	RAM	32	5.06
5									
6	Chip_A	2C014	CONF D	Data-ACQ (64KB)					
7	Chip_A	2C015	F-BLOCK 1	32 KB Guest ROM		1	ROM	32	5.06
8									

Because of F-Blocks 0 and 1 (aka SYSRAM area) are hardware write-protected you have to disable the protection with setting jumper CN2-4 before writing to that memory area. The red LED on the FRAM71B module should light up (see also the FRAM71B User Manual: <http://www.hpmuseum.org/forum/attachment.php?aid=3958> p. 10.P71B system.

Then deactivate the "Guest ROM" before switching to Bank 2 for the new ROM modules.

```

1 POKE "2C000","D3E4D5D69798191A9B000000" [ENTER] -> prevent a computer freeze
2                                     and/or a memory lost
3 or short POKE "2C012","000000"
4 [f] [OFF] [ON] -> Activate the configuration

```

Bank switching to Bank No 2

```

1 POKE "2C000","D3E4D5D69798191A9B109100" -> prepare as RAM
2 or short POKE "2C012","109100"
3 [f] [OFF] [ON] -> Activate the configuration

```

You should now see the new RAM configured as IRAM (Type 1). When you do not disable the write protect you will see this area as RAM (Type: 0).

CHECK configuration:

```

1 [SHOWPORT]
2
3 [RUN MEMBUF]
4 Port Dev Seq Size Addr Type
5 0.05 16384 2 0 0 0 4 60000 0
6 5 16384 2 FTH41 0 1 0 4 62000 0
7 5.01 32768 2 MATHROM 0 2 0 4 64000 0
8 5.02 32768 2 JPCF04 0 3 0 4 66000 0
9 5.03 32768 1 IRAM 1 5 5 0 96 30000 0 Main RAM
10 5.04 32768 1 IRAM 2 0 5 0 16 70000 2
11 5.06 65535 1 DATA-ACQ 5 0 0 16 78000 2 FTH41
12 0 4096 0 5 1 0 32 D0000 2 MATHROM
13 0.01 4096 0 5 2 0 32 C0000 2 JPCF04
14 0.02 4096 0 5 3 0 32 B0000 1 IRAM 1
15 0.03 4096 0 5 4 0 32 A0000 1 IRAM 2
16 5.05 98304 0 Main RAM 5 5 0 64 80000 1 DATA-ACQ
17 MEM [ENTER] -> You should have around 112 KB

```

Load ROM image file:

```
1 ROMCOPY DATAQ:TAPE TO :PORT(5.06);ROMSIZE=65536 [ENTER] -> copy DATAQ to new ROM
```

Remove IRAM identifier

```
1 PEEK$("80000",8) [ENTER] -> "B3DDDDDE" IRAM identifier
2 POKE "80000","00000000" [ENTER] -> Remove the IRAM identifier
3 PEEK$("80000",8) [ENTER] -> "00000000" validates the removal of the
4 IRAM identifier
```

Reconfigure module type

```
1 POKE "2C000","D3E4D5D69798191A9B50D100" [ENTER] -> Reconfigure RAM
2 from "D3E4D5D69798191A9B(1091)00" to ROM "D3E4D5D69798191A9B(50D1)00"
3 or short POKE "2C012","50D100"
4 [f] [OFF] [ON] -> Activate the configuration
```

CHECK configuration:

```
1 [SHOWPORT] [RUN MEMBUF]
2
3 Port Dev Seq Size Addr Type
4 0.05 16384 2 0 0 0 4 60000 0
5 5 16384 2 FTH41 0 1 0 4 62000 0
6 5.01 32768 2 MATHROM 0 2 0 4 64000 0
7 5.02 32768 2 JPCF04 0 3 0 4 66000 0
8 5.03 32768 1 IRAM 1 5 5 0 96 30000 0 Main RAM
9 5.04 32768 1 IRAM 2 0 5 0 16 70000 2
10 5.06 65535 2 DATA-ACQ 5 0 0 16 78000 2 FTH41
11 0 4096 0 5 1 0 32 D0000 2 MATHROM
12 0.01 4096 0 5 2 0 32 C0000 2 JPCF04
13 0.02 4096 0 5 3 0 32 B0000 1 IRAM 1
14 0.03 4096 0 5 4 0 32 A0000 1 IRAM 2
15 5.05 98304 0 Main RAM 5 5 0 64 80000 2 DATA-ACQ
MEM [ENTER] -> You should have around 112 KB
```

Finally activate write protect (J2-4) to avoid lighting the red LED on the FRAM71B.

Final validation

```
1 VER$ [ENTER] -> HP71:2CDCC FTH41:1A EDT:A MATH:1A JPC_F04 HPIL:1B RCPY:E
2 INST:A TCNV:A
```

If you don't have the HP3421A unit you can check the function ROM with following little program from the Data Acquisition Pac Owner's Manual (HP 82479A) section F-5 for the HP3421A:

```
1 10 SUB CHANLIST(B1,B2,C(),E)
2 20 DATA 2,2,2,2,2,2,2,2,0,0
3 30 DATA 3,3,1,1,1,1,1,1,1,1
4 40 DATA 3,3,1,1,1,1,1,1,1,1
5 50 FOR I=0 TO 29
6 60 READ C(I)
7 70 NEXT I
8 80 B1=2 @ B2=1 @ E=0
9 90 END SUB
```

```
1 RUN SETIP [ENTER]
2 Reading the HP3421 ...
3 Edit File Verify Quit?
```

6.9 Conventional Bank Switching

Take care of the whole process. Whenever you want to switch between the banks you have to deactivate the actual configuration and activate this step with OFF/ON. Same with activation of the new bank.

6.9.1 Activating the 16KB FINANCE and CIRCUIT ROM

Activating the 16KB FINANCE and CIRCUIT ROM in Bank 1 as IRAM (Chip No.0 with FRAM-Block No.3)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C0012","000000" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C012","EEEF00" [ENDLINE] -> activating bank No. 1 as selected ROMs
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5.06) [ENDLINE] // show port 5 FINANCE ROM content
4 CAT: PORT(5.07) [ENDLINE] // show port 5 CIRCUIT ROM content
```

6.9.2 Activating the 32KB CURVEFIT and AMPISTAT ROM

Activating the 32KB CURVEFIT and AMPISTAT ROM in Bank 2 as IRAM (Chip No.0 with FRAM-Block No.4)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost

```
1 POKE "2C012","000000" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C012","DCDD00" [ENDLINE] // activating bank No.1 as selected ROMs
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5.06) [ENDLINE] // show port 5 CURVEFIT ROM content
4 CAT :PORT(5.07) [ENDLINE] // show port 5 AMPISTAT ROM content
```

6.9.3 Activating the 64KB DATA-ACQ ROM

Activating the 64KB DATA-ACQ ROM in Bank 3 as IRAM (Chip No.0 and No.1 with FRAM-Block No.5)

Remove Chip No.0 configuration, to prevent a computer freeze or memory lost.

```
1 POKE "2C012","000000" [ENDLINE]
2 [OFF] [ON] -> Activate the configuration
```

```
1 POKE "2C012","50D100" [ENDLINE] // activating bank No.1 as selected ROMs
2 [OFF] [ON] -> Activate the configuration
3 CAT :PORT(5.06) [ENDLINE] // show port 5 DATA-ACQ ROM content
```