

B. Tech Degree III Semester Examination, November 2008

CS 302 LOGIC DESIGN

(2006 Scheme)

Time : 3 Hours

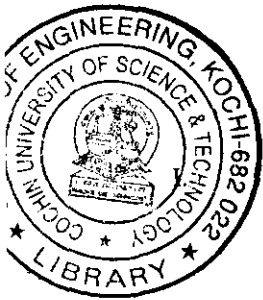
Maximum Marks : 100

PART A

(Answer ALL questions)

(Each question carries FIVE marks)

(8 x 5 = 40)



- (a) Express the Boolean function $F = xy + \bar{x}z$ in a product of max terms form.
- (b) Explain De-morgan's Laws.
- (c) Implement a Boolean function $F(a, b, c, d) = \sum(0, 1, 3, 4, 8, 9, 15)$ with multiplexer.
- (d) Draw the PLA block diagram and explain its features.
- (e) Write a short note on Excitation Tables.
- (f) Write a short note on state table of a sequential circuit.
- (g) What is meant by Noise Margin?
- (h) Write the features of CMOS logic devices.

PART B

- II. (a) Simplify the following Boolean function by using K.map method.

$$F = \sum(0, 1, 2, 8, 10, 11, 14, 15)$$
 (6)
 - (b) Find the complement of the function.

$$F = \bar{x}y\bar{z} + \bar{x} \bar{y}z$$
 (3)
 - (c) Minimise the logic function in POS form

$$F(A, B, C, D) = \pi M(4, 6, 10, 12, 13, 15).$$
 (6)

OR
- III. (a) Simplify the Boolean function

$$F = \bar{A}\bar{B}\bar{C} + \bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}$$
 (6)
 - (b) Explain the postulates and theorems of Boolean Algebra. (6)
 - (c) Write a short note on **Don't care conditions**. (3)
- IV. (a) Implement the basic gates using Universal gates? Write the algebraic derivation also. (5)
 - (b) Derive and draw the complete logic diagram for 4 bit full adder with look ahead carry. (10)

OR
- V. (a) Determine the prime implicants of the function

$$F(w, x, y, z) = \sum(1, 4, 6, 7, 8, 9, 10, 11, 15)$$
 (10)
 - (b) Implement a full adder circuit with a decoder and two OR gates. (5)
- VI. (a) Differentiate between combinational and sequential circuits. (5)
 - (b) Design a mod - 9 synchronous down counter using J.K Flip Flop. (10)

OR
- VII. (a) What is meant by asynchronous inputs Flip Flops? (5)
 - (b) Design and explain a 4 bit up-down binary counter. (10)
- VIII. (a) Draw and explain the circuit for a TTL gate with Totem Pole output driver? (7)
 - (b) Explain 2 input CMOS NOR gate and 2 input CMOS NAND gate in detail. (8)

OR
- IX. Describe in detail, how can interface the CMOS and TTL logic family devices with the help of figures. (15)