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B. Tech Degree III Semester Examination November 2011

CS 302 LOGIC DESIGN

(2006 Scheme)

Time : 3 Hours Maximum Marks : 100

PART A

(Answer ***ALL*** questions)

(8 x 5 = 40)

I. (a) (i) $(A72B)_{16} = (\ )_8$

(ii) $(1100\ 1111\ 0101)_2 = (\ )_{16}$

(iii) $(0001\ 0100\ 0111\ 0101)_{BCD} = (\ )_{10}$

(iv) $(74.562)_8 = (\ )_2$

(v) $(2479)_{10} = (\ )_{16}$

(b) Explain Demorgan's Theorem.

(c) Distinguish between PLA and PAL architecture.

(d) Implement $(A+BC)(B+\bar{A}C)$ using minimum number of logic gates.

(e) Explain Karnaugh map representation and simplification of expressions.

(f) Design a full adder using NAND gates.

(g) Distinguish between CMOS and TTL families.

(h) Write notes on:

(i) fan in and fan out

(ii) power dissipation

PART B

(4 x 15 = 60)

II. (a) Convert SOP to POS and POS to SOP expressions with examples. (10)

(b) Explain Gray code and Excess – 3 code. (5)

OR

III. (a) Explain 1's and 2's complement arithmetic with examples. (5)

(b) Reduce the expression $\sum m(0,1,2,3,5,7,8,9,10,12,13)$ and implement using minimum number of NAND gates only and NOR gates only. (10)

IV. (a) Explain the concept of a carry look ahead adder. (5)

(b) Design a BCD to hexadecimal converter. (10)

OR

V. (a) Explain how a 3 bit counter can be implemented using multiplexer. (8)

(b) Design a switching circuit to generate odd parity bits for decimal number expression in BCD code. (7)

VI. (a) Convert a JK flip flop into T flip flop. Give the truth table and logic diagrams. (5)

(b) Design and explain Johnson and Ring counters. (10)

OR

VII. (a) Compare combinational and sequential circuits. (5)

(b) Design and implement a decimal up down counter with a mode control (10)

VIII. (a) Explain Tristate Logic. (5)

(b) Explain the interfacing between CMOS and TTL gates. (10)

OR

IX. (a) Write notes on:

(i) noise margin

(ii) propagration delay

(iii) speed power relation (6)

(b) Compare the characteristics of DTL, RTL and TTL gates. (9)

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