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# END-TERM EXAMINATION

FOURTH SEMESTER [B.TECH.] - MAY 2008

Paper Code: ETEC206

Subject: Digital Circuits and System-I

Paper ID: 28206

(Batch: 2004-2006)

Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions.

- Q.1 (a) Convert the following binary fractions into binary-weighted fractions. (5)  
 (i) 1.01 (ii) 0.101
- (b) Convert the following binary number into (i) gray code (ii) excess-3 code. (5)  
 (1) 1011 (2) 11100
- (c) Simplify  $S = \Sigma (0, 1, 2, 5, 7, 9, 10) + d (3, 8, 15)$  where d denotes don't care terms. (5)
- Q.2 (a) Implement the following functions using NAND gates only (5)  
 (i)  $Y = abc + \bar{b}c\bar{d}$  (ii)  $Y = a + b(c + d)$
- (b) Obtain a 3 x 1 MUX from a 4 x 1 MUX. Compare electronic multiplexer and mechanical multiplexer. (10)
- Q.3 (a) What is a decoder? Implement the following using Demux/Decoder. (8)  
 (i)  $\Sigma (0, 1, 3, 4, 8, 9, 10)$   
 (ii)  $\Sigma \bar{a}\bar{b}\bar{c} + a\bar{b}c + abc\bar{d} + abc\bar{d}$
- (b) Construct binary to 7 segment converter. (7)
- Q.4 (a) Prove that a full adder is equal to the sum of two half adders. (8)  
 (b) Describe the operation of look-ahead carry adder. What are its advantages over ordinary adder? (7)
- Q.5 (a) Compare synchronous and asynchronous sequential logic circuits. (5)  
 (b) What is the race-around problem and how it is rectified? (5)  
 (c) Convert J-K flip flops to S-R and D flip flops. (5)
- Q.6 (a) What is Johnson counter? How can you use it as a 2N:1 counter? (8)  
 (b) Explain working of successive approximation ADC. (7)
- Q.7 (a) Explain the features of following logic families. (8)  
 (i) DTL (ii) ECL (iii) TTL (iv) CMOS
- (b) Compare and contrast RAM, ROM and CAM. (7)
- Q.8 Write short notes (any three): - (15)
- (a) PLA  
 (b) Mealy and Moore Machine  
 (c) Nyquist Sampling  
 (d) Comparator  
 (e) Astable multi-vibrator

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